REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 3, 4, 6-8, 11, 12 and 18-20 are presently pending in this application, and Claim 1 is amended by way of the present amendment.

In the outstanding Office Action, Claim 1-4, 7-8, 11, 18-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 6,687,985 to Sakamoto et al. in view of U.S. 5,541,450 to Jones et al.; Claims 6 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Jones et al., and further in view of U.S. 5,963,430 to Londa.

Turning now to the merits, in order to expedite issuance of a patent in this case, Claim 1 is amended to clarify datentable distinctions of the present invention over the cited references. Specifically, amended Claim 1 recites a multi-layer printed wiring board including a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate, and a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board. The second substrate has a continuous metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the continuous metallic layer portion such that the plurality of non-through holes are electrically connected to each other. Also recited is an IC component having a terminal side including a plurality of terminals, and a non-terminal side which is opposite to the terminal side. The IC component is loaded in the opening of the first substrate such that the non-terminal side of the IC component contacts the metallic layer portion and the terminals of the IC component face outward of the opening in the first substrate. The IC

component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component.

Thus, Claim 1 is amended to clarify that the second substrate has ***a continuous metallic layer portion in the opening of the first substrate*** and a plurality of non-through holes filled with conductive material and connected to the continuous metallic layer portion ***such that the non-through holes are electrically connected to each other***. An example of this configuration is shown in Figs. 1 and 2 of Applicants specification. As seen in these Figures, the metal layer 28a is a continuous layer provided in contact with the non-terminal side of the IC component 70, and also contacts the non-through holes 18a in the second substrate so that these non-through holes are electrically connected. The continuous metal layer 28a and the non-through holes irradiate heat away from the IC 70. Thus, heat generated by the IC component is effectively radiated to and removed through the metallic layer portion and the non-through holes, thereby preventing heat damage caused by the IC component.

Sakamoto et al. discloses a carrier board 16 set in a cavity 15 of a mother board 11 and electrically connected to the mother board 11. As seen in Fig. 1 of Sakamoto et al., the carrier board includes a plurality of discrete electrodes 21 provided on a first side for connecting to respective discrete electrodes 22 of the mother board. That is, the electrodes 22 do not provide a continuous metal layer that electrically connect the through-holes in the mother board 11.

Thus, Sakamoto et al. does not disclose the second substrate having a continuous metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the continuous metallic layer portion such that the non-through holes are electrically connected to each other, as now required by amended Claim 1. In this regard, Applicants submit there is no indication in Sakamoto et al. that the via-hole conductors 14 are configured to irradiate heat from the carrier board. As

such, Sakamoto et al. also fails to disclose that the carrier board is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the carrier board, as also required by Claim 1.

Jones et al. cannot correct the above-deficiencies of Sakamoto et al. As seen in the figures of Jones et al., a semiconductor die 18 is attached by way of an attach pad 36 to a support substrate 32. Although the metal layer 36 is continuous, it is not connected to any vias or other structure in the support board 36 for irradiating heat from the die 36. In fact, Applicants submit that Jones et al. does not provide any structure (other than the support 32 itself) in contact with the non terminal side of the die 18.

Thus, even if combined, the combination of Sakamoto et al. and Jones et al. does not disclose the second substrate having a ***continuous metallic layer*** portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material ***and*** connected to the continuous metallic layer portion such that ***the non-through holes are electrically connected to each other***, as now required by amended Claim 1.

Moreover, Applicants submit that one of ordinary skill in the art would not find it obvious to combine the die 18 and die attach pad 36 of Jones et al. within the opening of the motherboard in Sakamoto et al. As noted above, the opening in Sakamoto et al. includes discrete contacts 22 for accommodating the terminals of the carrier. Thus, if the attach pad 36 is used in Sakamoto et al., it would short the contacts 22 and render the motherboard completely inoperable. This provides another reason for the patentability of amended Claim 1 over the cited references.

Finally, Londa is cited for teachings of conductive bumps and is not believed to teach or suggest the features absent from Sakamoto et al. and Jones et al. as noted above.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 3, 4, 6-8, 11, 12 and 18-20 depend directly or indirectly from Claim 1, substantially

the same arguments set forth above also apply to these dependent claims. Hence, Claims 3, 4, 6-8, 11, 12 and 18-20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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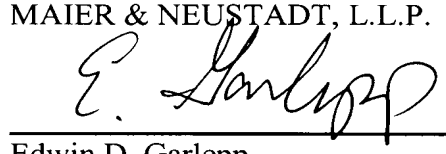

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